

Figure 1A

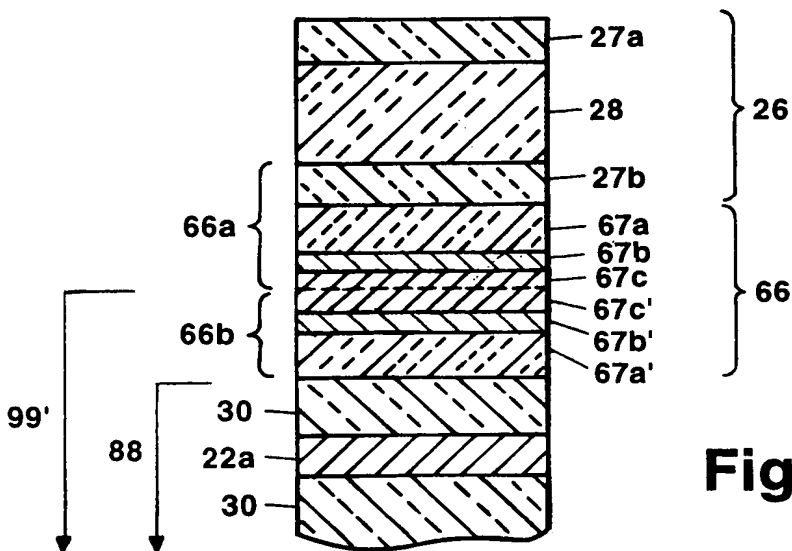


Figure 1B



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

2/9

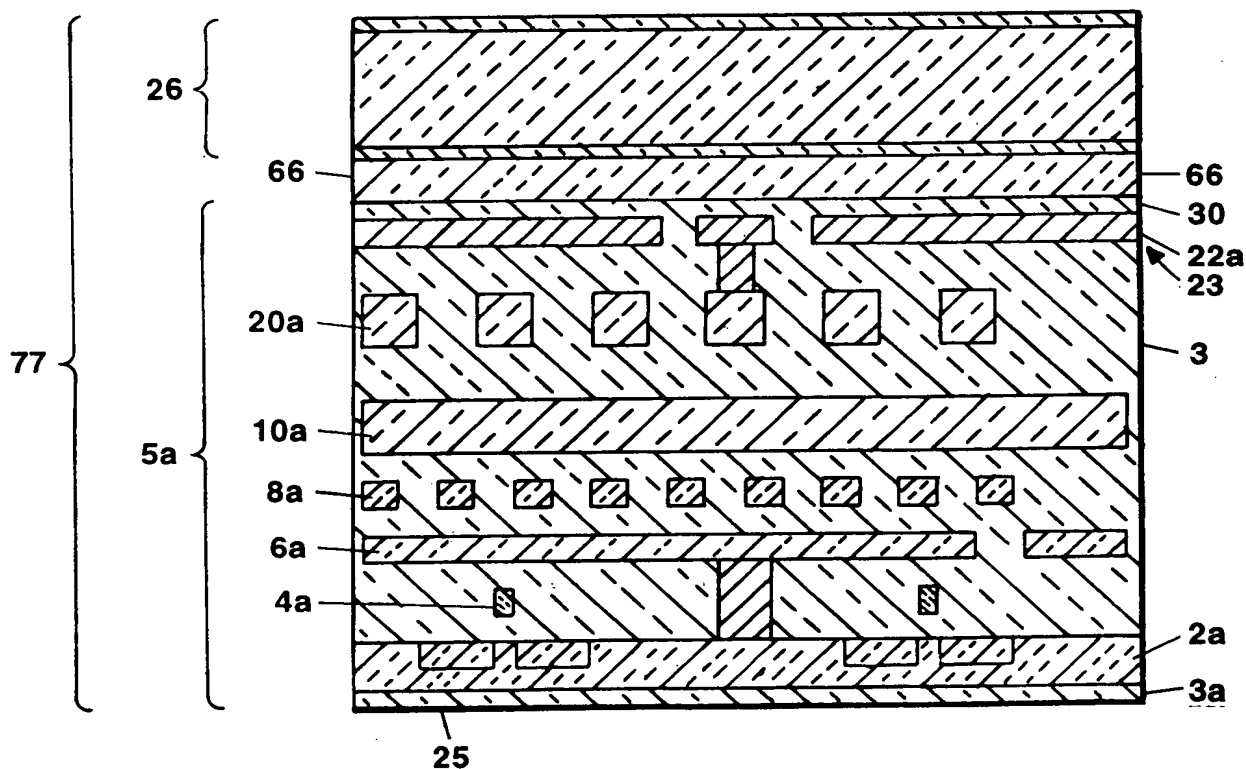
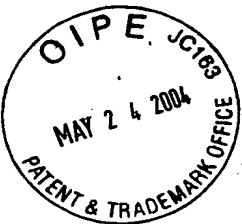


Figure 2A



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

3/9

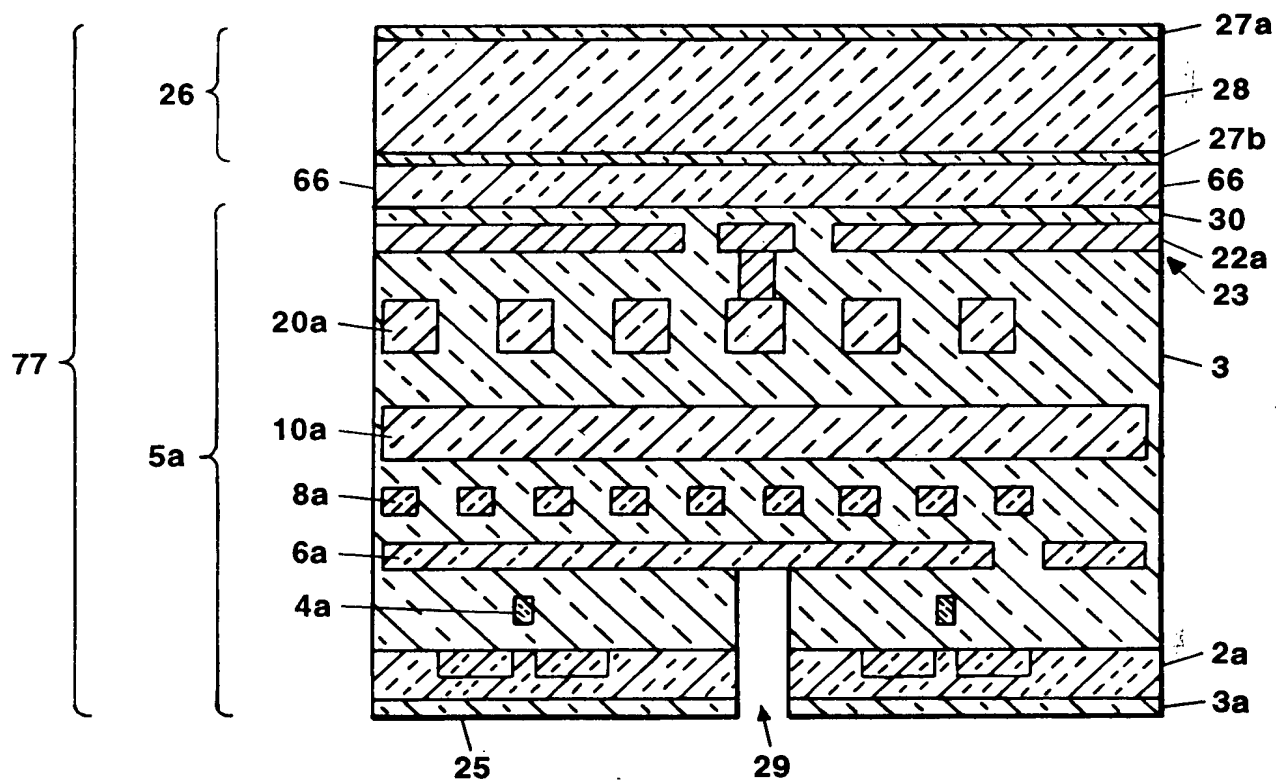


Figure 2B



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

4/9

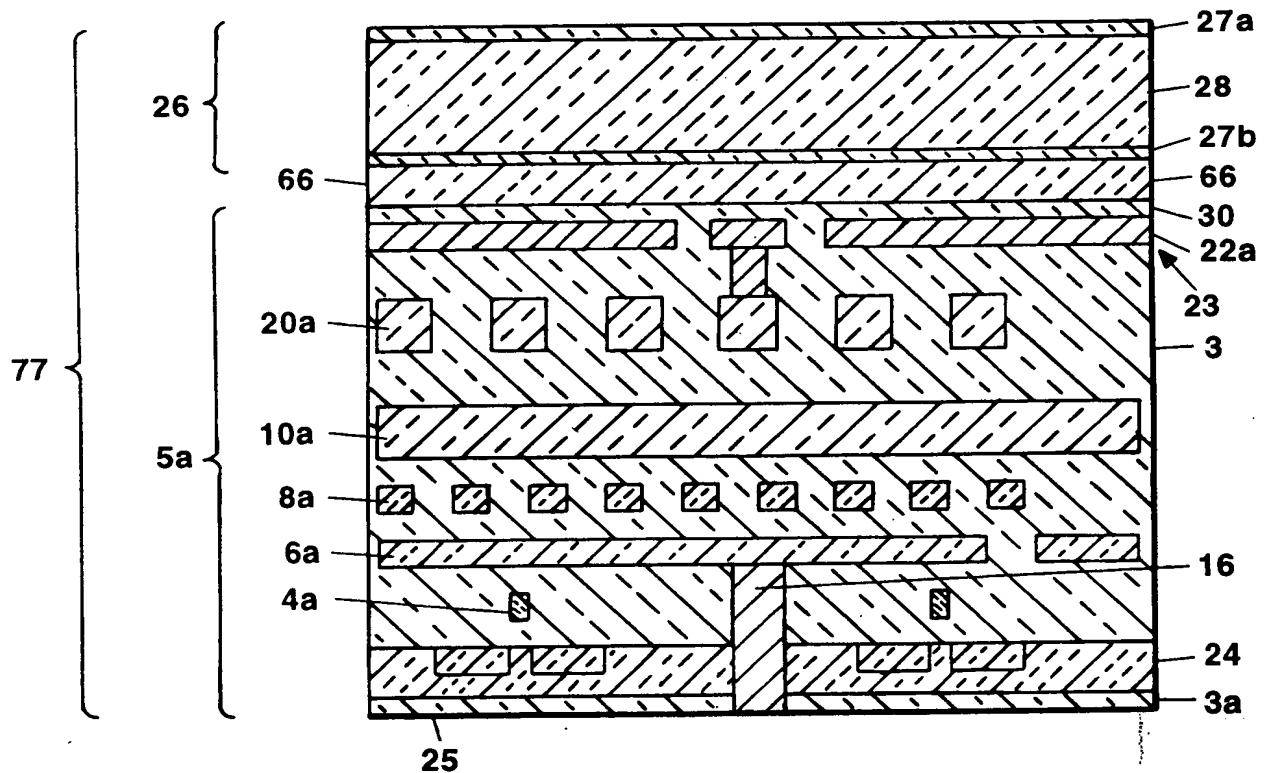


Figure 2C



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

5/9

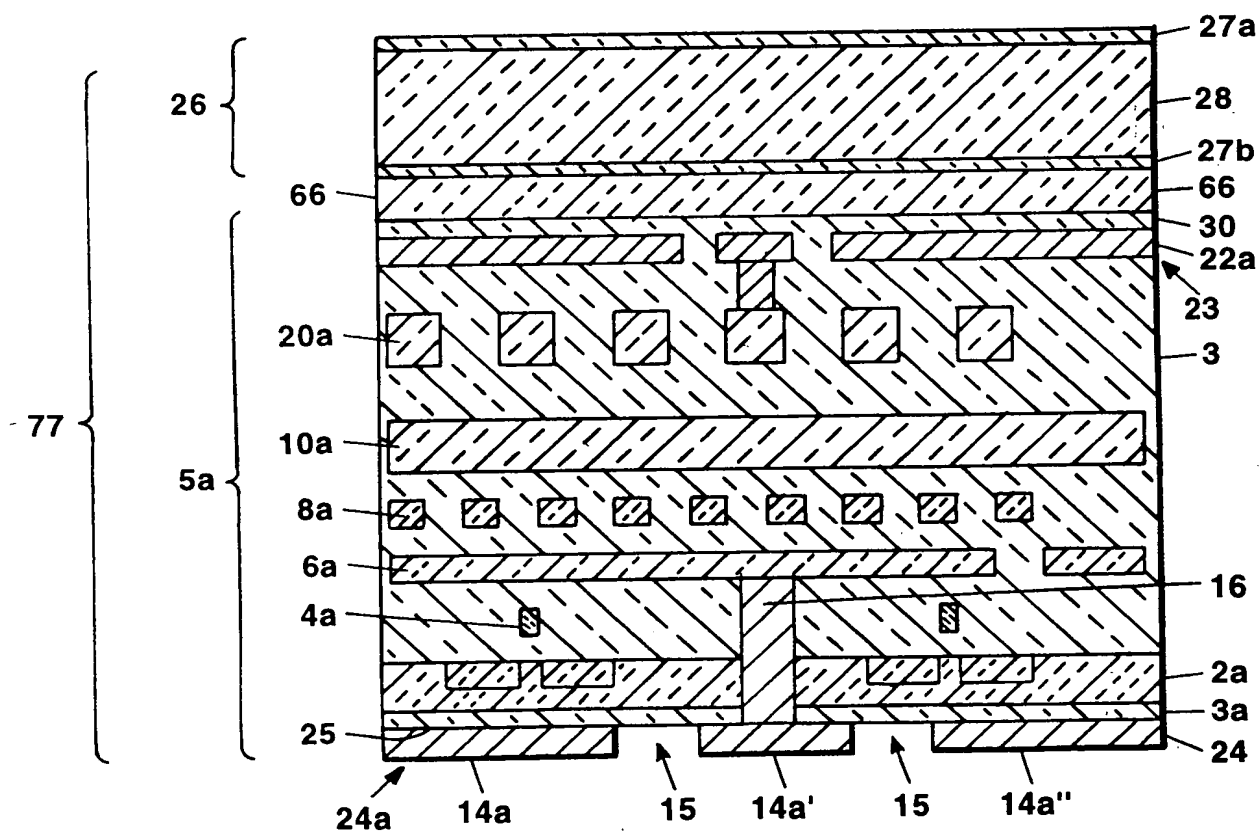


Figure 2D



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

6/9

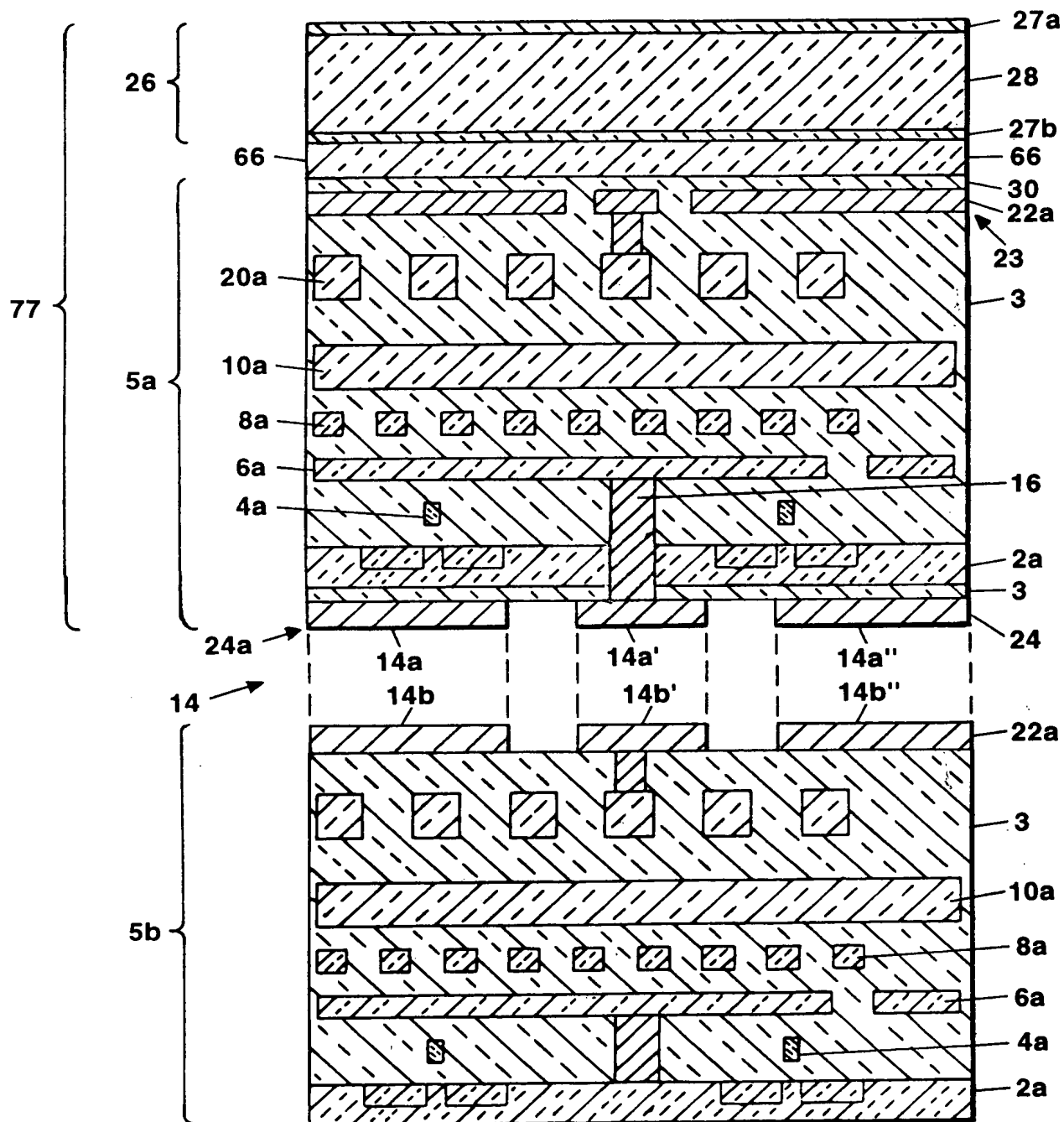


Figure 3A



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

7/9

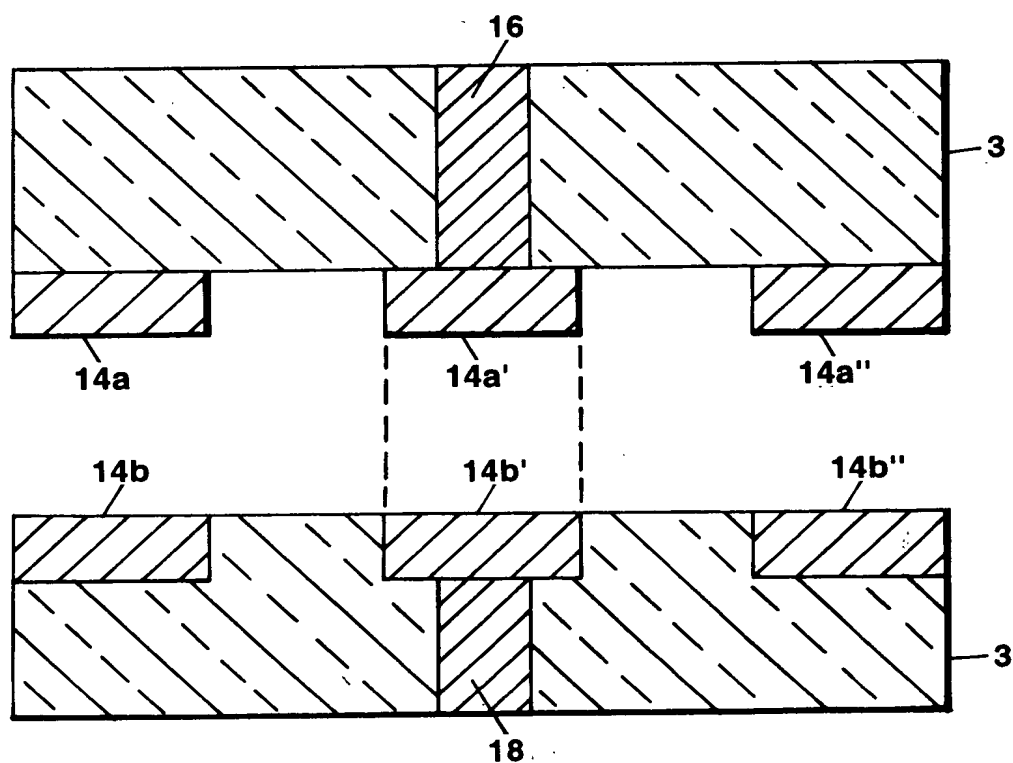


Figure 3B

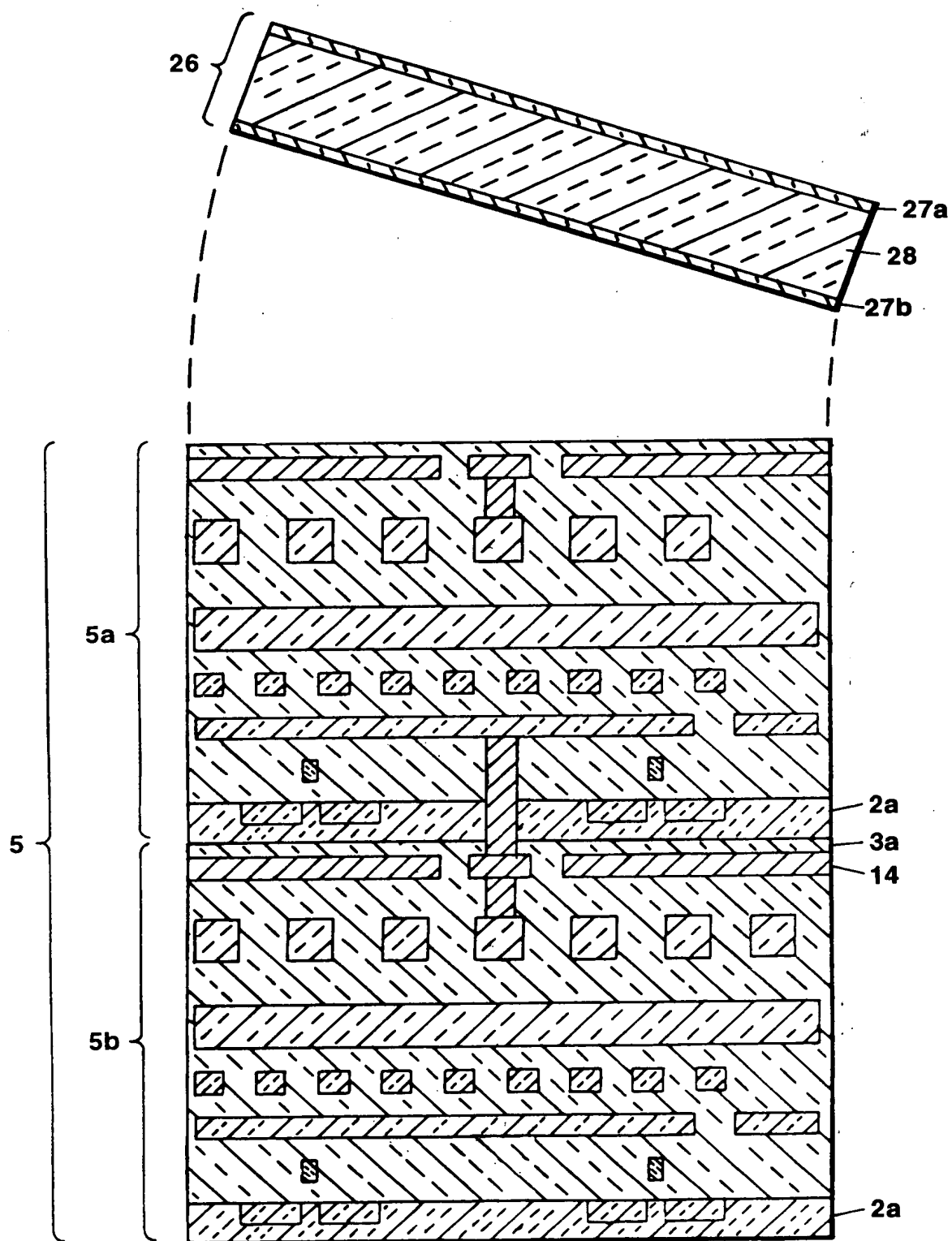


Figure 4A



METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE INCORPORATING A
PROCESSING HANDLE MEMBER

Rafael Reif, et al.
Application No. 10/749,103

9/9

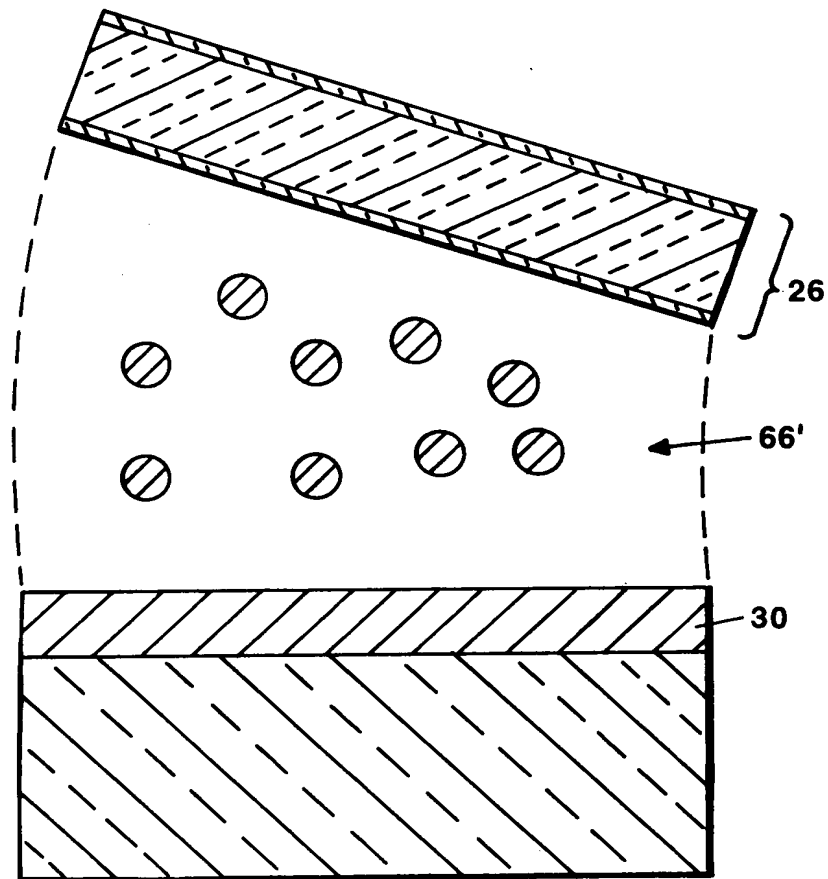


Figure 4B